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Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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08/082,328 06/24/93 KNIGHT

T 7828003

EXAMINER

MMC2/0326

PENNIE & EDMONDS  
1155 AVENUE OF THE AMERICAS  
NEW YORK NY 10036-2711

VIGUSHIN, J ART UNIT	PAPER NUMBER
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2841  
DATE MAILED:

03/26/01

**Please find below and/or attached an Office communication concerning this application or proceeding.**

**Commissioner of Patents and Trademarks**

08/04/25 28



UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
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EXAMINER
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ART UNIT	PAPER NUMBER
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DATE MAILED:

45

This is a communication from the examiner in charge of this application  
COMMISSIONER OF PATENTS AND TRADEMARKS

### NOTICE OF ALLOWABILITY

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance and Issue Fee Due or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

☒ This communication is responsive to APPEAL BRIEF filed January 10, 2001

☒ The allowed claim(s) is/are 1, 28, 37-48, 52-59, 102, 143, 144, 146 and 147

☐ The drawings filed on \_\_\_\_\_ are acceptable as formal drawings.

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

☐ All ☐ Some\* ☐ None of the:

☐ Certified copies of the priority documents have been received.

☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_

☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\*Certified copies not received: \_\_\_\_\_

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. THIS THREE-MONTH PERIOD IS NOT EXTENDABLE FOR SUBMITTING NEW FORMAL DRAWINGS, OR A SUBSTITUTE OATH OR DECLARATION. This three-month period for complying with the REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL is extendable under 37 CFR 1.136(a).

☐ Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION, PTO-152, which discloses that the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.

☒ Applicant MUST submit NEW FORMAL DRAWINGS

☐ because the originally filed drawings were declared by applicant to be informal.

☒ including changes required by the Notice of Draftperson's Patent Drawing Review, PTO-948, attached hereto or to Paper No. 16

☐ including changes required by the proposed drawing correction filed on \_\_\_\_\_, which has been approved by the examiner.

☐ including changes required by the attached Examiner's Amendment/Comment or in the Office action of Paper No. 16

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings.

☐ Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Any reply to this notice should include, in the upper right hand corner, the APPLICATION NUMBER (SERIES CODE/SERIAL NUMBER). If applicant has received a Notice of Allowance and Issue Fee Due, the ISSUE BATCH NUMBER and DATE of the NOTICE OF ALLOWANCE should also be included.

#### Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s) 8 and 43

☐ Notice of Draftperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

☒ Interview Summary, PTO-413

☒ Examiner's Amendment/Comment

☐ Examiner's Comment Regarding Requirement for the Deposit of Biological Material

Statement of Reasons for Allowance

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### DETAILED ACTION

#### *Response to Appeal Brief*

1. The present Office Action is responsive to Applicant's Appeal Brief filed January 10, 2001. The status of the claims is as follows: Claims 29, 80-101, 201 and 202 were canceled in Applicant's Response to Restriction Requirement filed June 14, 1995 (Paper No. 12). Claims 2-27, 30-36, 49-51, 60-79, 103-142, 145, 148-200 and 203-209 were canceled in Applicant's Preliminary Amendment filed November 05, 1998 (Paper No. 28). Claims 1, 28, 37-48, 52-59, 102, 143, 144, 146 and 147 are now pending in the instant Application.
2. Applicant's arguments filed in the above-cited Appeal Brief have been fully considered and deemed persuasive.

#### *Examiner's Amendment*

3. The following amendments correct informalities in the Specification and cure a 35 USC §112 ¶2 defect in Claim 59 in order to place the instant Application in condition for allowance. These amendments have been authorized by Applicant's Attorney, Francis E. Morris, in telephone conversations conducted on March 13, 2001 and March 21, 2001.

##### *In the Specification:*

On p.22, line 26: "Fig. 6 depicts" has been changed to --Figs. 6A-D depict--.

On p.23, between lines 24 and 25, the following Drawing descriptions have been inserted:

--Fig. 17A depicts a perspective view of a prior art face-up level 1 package.

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Fig. 17B depicts an exploded view of a flip-chip level 1 modular system

implemented in accordance with the invention.--

On p. 24, line 10: "present" has been changed to --prior--.

In the Claims:

Unmarked version:

22  
59. (Examiner's Amendment) A modular electronic system comprising:  
a substrate;  
a chip;  
means for powering said chip;  
means for capacitively signaling between said chips and said substrate  
comprising first and second coupled half-capacitors, said first half-capacitor being associated with  
said chip and said second half-capacitor being associated with said substrate, said first and second  
coupled half-capacitors comprising effectively overlapping conductive regions separated by a gap;  
and an additional half-capacitor associated with one of said chip and said substrate.

Marked-up version showing changes:

59. (Examiner's Amendment) A modular electronic system comprising:  
a substrate;  
a chip;  
means for powering said chip;

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means for capacitively signaling between said chips and said substrate comprising first and second coupled half-capacitors, said first half-capacitor being associated with said chip and said second half-capacitor being associated with said substrate, said first and second coupled half-capacitors comprising effectively overlapping conductive regions separated by a gap; and an additional half-capacitor [on its backside] associated with one of said chip and said substrate.

***Information Disclosure Statement***

4. The Examiner acknowledges the receipt (on March 14, 2001) and entry into the file (as Paper No. 43) of the non-patent literature cited in the PTO-Form 1449 listings of IDS Paper Nos. 8 (filed November 03, 1993) and 29 (filed November 05, 1998). The above-cited non-patent literature has now been reviewed, along with the other prior art of record, in conjunction with the Applicant's Appeal Brief arguments, and the pending Claims have been deemed allowable over the prior art of record.

5. Enclosed with the present Office Action are copies of Applicant's PTO-1449 Forms from IDS Paper Nos. 43 and 8, initialed, signed and dated by the present Examiner. The PTO-1449 Form from IDS Paper No. 29 had already been initialed, signed, dated and mailed by the previous Examiner (Donald A. Sparks).

***Allowable Subject Matter***

6. Claims 1, 28, 37-48, 52-59, 102, 143, 144, 146 and 147 have been allowed.

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7. The following is an examiner's statement of reasons for allowance:

Regarding Claims 1, 37-43, 45-48 and 52-58, patentability resides, at least in part, in **the combination of: *means for capacitively signalling*** (defined on p.25, lines 21-25 in the Specification and on p.4 of Applicant's Appeal Brief) ***between the chip and the substrate and signal leads connected on the substrate and the chip to the means for capacitively signalling***, in further combination with the other limitations of base Claim 1.

Regarding Claim 28, patentability resides, at least in part, in **the combination of: *a signal lead of at least one of the plurality of electronic devices coupled to a first half-capacitor attached to the chip and a second half-capacitor attached to the substrate and capacitively coupling a signal to the first half-capacitor***, in further combination with the other limitations of the claim.

Regarding Claim 44, patentability resides, at least in part, in ***the power connector extending through the claimed dielectric***, in combination with the other limitations of the claim.

Regarding Claim 59, patentability resides, at least in part, in ***an additional half-capacitor associated with one of said chip and said substrate***, in combination with the other limitations of the claim.

Regarding Claims 102, 143, 144, 146 and 147, patentability resides, at least in part, in ***at least one signal lead connecting the electronic devices of the first module to the first half-capacitor and the first and second half-capacitors providing a capacitive signal path between the first and second modules***, in combination with the other limitations of base Claim 102.

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8. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

9. Claims 1, 37-43, 45-48, 53-58, 52, 28, 44, 59, 102, 143, 144, 146 and 147 of the instant allowed Application will be renumbered as Claims 1-27, respectively, for publication in the issued patent.

### *Conclusion*

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following references disclose decoupling capacitors between power and ground layers:

Turek (US 4,775,573): col.5: 19-23.

Herrero et al. (US 4,675,717): col.4: 21-28.

Hayes et al. (US 4,642,569): col.5: 26-29 and 40-45.

Marshall et al. (US 4,605,915): col.5: 19-col.6: 27.

Suzuki (US 4,640,866) discloses a circuit board comprising insulating layers having material composition (i.e., PTFE) which provides the circuit board with excellent high frequency transmission characteristics and a small thermal expansion coefficient (col.4: 15-28).

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McMonagle (US 4,633,035) discloses a circuit board comprising a laminate structure of a dielectric sheet (PTFE) with a thin layer of copper on one surface and a thicker layer of aluminum on the other surface, and through-holes drilled in said laminate structure. The laminate structure and materials used therefor provide a circuit board suitable for use at microwave frequencies (col.1: 10-16; col.2: 24-57).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John Vigushin whose telephone number is (703) 308-1205. The examiner can normally be reached on Monday to Friday from 8:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Gaffin, can be reached on (703) 308-3301. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7382.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

John B. Vigushin  
Patent Examiner  
March 22, 2001

  
**Jayprakash N. Gandhi**  
**Primary Examiner**  
**Technology Center 2800**

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UNITED STATES DEPARTMENT OF COMMERCE  
Patent and Trademark Office

**NOTICE OF ALLOWANCE AND ISSUE FEE DUE**

MMC2/0326

PENNIE & EDMONDS  
1155 AVENUE OF THE AMERICAS  
NEW YORK NY 10036-2711

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
08/082,328	06/24/93	27	VIGUSHIN, J 2841	03/26/01
First Named Applicant	KNIGHT, 35 USC 154(b) term ext. = 0 Days.			

TITLE OF INVENTION: METHOD AND APPARATUS FOR NON-CONDUCTIVELY INTERCONNECTING INTEGRATED CIRCUITS

ATTYS DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
7828003	361-782.000	209	UTILITY	YES	\$620.00	06/26/01

**THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED.**

**THE ISSUE FEE MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED.**

**HOW TO RESPOND TO THIS NOTICE:**

I. Review the SMALL ENTITY status shown above.  
If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

- A. If the status is changed, pay twice the amount of the FEE DUE shown above and notify the Patent and Trademark Office of the change in status, or
- B. If the status is the same, pay the FEE DUE shown above.

If the SMALL ENTITY is shown as NO:

- A. Pay FEE DUE shown above, or
- B. File verified statement of Small Entity Status before, or with, payment of 1/2 the FEE DUE shown above.

II. Part B-Issue Fee Transmittal should be completed and returned to the Patent and Trademark Office (PTO) with your ISSUE FEE. Even if the ISSUE FEE has already been paid by charge to deposit account, Part B Issue Fee Transmittal should be completed and returned. If you are charging the ISSUE FEE to your deposit account, section "4b" of Part B-Issue Fee Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give application number and batch number.  
Please direct all communications prior to issuance to Box ISSUE FEE unless advised to the contrary.

**IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.**

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